

A1
Because the tag 14 only enables the PLL after examining a portion of the FLP, the amount of time the tag PLL is ON is minimized. Therefore, packet interleaving in this fashion preserves tag battery power by minimizing the amount of time the PLL is ON when no valid FLPs that require a response are present (which could be a long period of time in the case of a fixed gate reader).

IN THE CLAIMS:

Please add new claims 142-197 as attached: